ABSTRACT OF THE DISCLOSURE

The present invention provides a CMOS imager with a reset scheme, by which a CMOS imager generates a sub-kTC noise so that read noise does not depend on the sense node capacitance. By using a column feedback circuit, reset noise can be suppressed to a negligible amount so that photogate APS or CCD-like circuits can achieve noise performance to very efficient value. This scheme allows increasing sense node capacitance without increasing the noise and also achieves a large full-well value without sacrificing read noise performance. The feedback circuit in one of the embodiment of the present invention is located at the column side of the circuit. This design provides a minimal change to the pixel. As a result quantum efficiency or pixel size is not compromised. The present invention allows a CMOS imager to capture scene with high intra-scene contracts under low illumination with high dynamic range.